REMARKS

Applicant has amended the Abstract, such that the Abstract is more descriptive of a test bus architecture.

Claims 1-10 have been rejected under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement. Support for "an integrated circuit chip" that includes a test bus architecture is found in the specification as originally filed at paragraph [0017]. Furthermore, Applicant does not see how the recitation of "an integrated circuit chip" can be indefinite. Certainly, one of ordinary skill in the art is reasonably appraised of "an integrated circuit chip". For these reasons, Applicant is not amending Claims 1-10 at this time.

Claim 4, which depends indirectly from Claim 1, has been rejected under 35 U.S.C. 112, second paragraph, as having no antecedent basis for "a plurality of RAM blocks". However, Claim 1 recites "a plurality of random access memory (RAM) blocks", thereby providing proper antecedent basis for "a plurality of RAM blocks" as recited in Claim 4. For these reasons, Claim 4 meets the requirements of 35 U.S.C. 112, second paragraph.

Claims 1-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal (U.S. Patent No. 5,568,437).

Claim 1 recites "a plurality of random access memory (RAM) blocks" and "a plurality of test modules, each being coupled to a corresponding one of the RAM blocks".

In contrast, Jamal teaches "An integrated circuit with a random access memory (RAM) and a built-in self tester for the RAM". (Jamal, Abstract.) The deficiencies of a built-in self tester (BIST) are described in Applicant's specification at paragraph [0002]. More specifically, paragraph [0002] states:

> Relatively large RAMs (i.e., 2Mb or larger) typically have a dedicated built-in self test (BIST) unit, which writes a predetermined bit pattern to the RAM. The contents of the RAM are then read and compared with the predetermined bit pattern to determine whether the RAM includes any defective memory cells. Because of the overhead associated with the BIST circuitry, this technique is only used for relatively large RAMs. Moreover, because BIST circuitry only provides a predetermined bit pattern for testing the RAM, the testing of the RAM may be inadequate because of a limited bit pattern. Furthermore, stress tests, in which the operating speed of the RAM is tested, cannot be readily performed using BIST circuitry.

Jamal describes one example of a BIST unit and a corresponding RAM as described in paragraph [0002]. Thus, Jamal fails to teach "a plurality of random access memory (RAM) blocks" and a corresponding "plurality of test modules" as recited by Claim 1.

The Examiner argues that "Jamal does not explicitly point out to multiplication (integration) of the elements, but Jamal does not limit such well known feature, inherently teaching for using any degree of element integration inside the chip".

However, not limiting a feature is not the same as teaching or suggesting the feature. In addition, the Applicant does not believe that the "multiplication" of BIST circuits is a "well known feature" as suggested by the Examiner. BIST circuits have a significant associated overhead (See, e.g., paragraph [0002]), which renders the use of multiple BIST circuits inefficient.

In addition, Jamal teaches that the BIST 100 is coupled to 10 pins of the integrated circuit (Fig. 2a). Thus, a "multiplication" of the BIST circuit 100 would require 10

addition pins for each additional BIST on the integrated circuit.

Alternately, Jamal teaches that "the BIST 100 is used in conjunction with a TAP interface 92" which requires 5 pins of the integrated circuit. (Jamal, Col. 4, lines 56-60; Fig 2b.) Thus, a "multiplication" of the BIST circuit 100 in this case would require an additional TAP interface and 5 addition pins for each additional BIST on the integrated circuit.

For these reasons, it would not be obvious to simply multiply the BIST circuit 100 and RAM block 84 taught by Jamal. Consequently, Jamal fails to teach or suggest "a plurality of random access memory (RAM) blocks" and "a plurality of test modules, each being coupled to a corresponding one of the RAM blocks" as recited by Claim 1.

In addition, Claim 1 recites "a dedicated test bus coupled to each of the test modules". Simply multiplying the BIST circuit 100 and RAM block 84 described by Jamal would result in a plurality of test buses, each coupled to a corresponding BIST circuit and RAM block. Thus, Jamal also fails to teach or suggest "a dedicated test bus coupled to each of the test modules" as recited by Claim 1.

For the above-described reasons, Claim 1 is allowable over Jamal. Claims 2-10, which depend from Claim 1, are allowable over Jamal for at least the same reasons as Claim 1.

In addition, Claim 8 recites "wherein each of the test modules comprises a register for storing a unique address". Because Jamal fails to teach more than one BIST circuit, Jamal necessarily fails to teach "each of the test modules comprises a register for storing a unique address". For this additional reason, Claim 8 is allowable over Jamal.

Claims 10-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal in view of Grider et al. (U.S. Patent No. 5,515,540).

Claim 10, which depends from Claim 1, is allowable over Jamal for at least the same reasons as Claim 1. Grider et al. fail to remedy the deficiencies of Jamal. Thus, Claim 10 is allowable over Jamal in view of Grider et al.

In addition, Claim 10 recites "wherein each of the RAM blocks has a capacity of 32 Kb or less".

The Examiner concludes that it would have been obvious to one by using a RAM with a limited capacity, because one of ordinary skill in the art would easier use the smaller RAM's capacity in order to achieve higher reliability.

However, as described in the specification as originally filed, RAM blocks having a capacity of 32 kb or less do not typically include associated BIST circuitry. (Specification, paragraph [0005].) As a result, RAM blocks of this size are typically not tested, or are tested with significant difficulty. (Specification, paragraph [0003].) Thus, contrary to the Examiner's assertion, it would not be obvious to use "a RAM with a limited capacity". For this additional reason, Claim 10 is allowable over Jamal in view of Grider et al.

Claim 11 recites "A method of operating RAM blocks having a capacity less of 32 Kb or less embedded in system circuitry on an integrated circuit chip". As described above in connection with Claim 10, Jamal and Grider et al. fail to teach or suggest the use of RAM blocks having a capacity of 32 Kb or less." As described above in connection with Claim 1, Jamal fails to teach or suggest the use of more than one RAM block. For these reasons, Claim 11 is allowable over Jamal in view of Grider et al.

In addition, Claim 11 recites "accessing the RAM blocks through a dedicated test bus during a test mode to test the functionality of the RAM blocks prior to normal operation of the chip". As described above in connection with Claim 1, Jamal fails to teach or suggest a dedicated test bus as recited by Claim 11. Thus, Jamal necessarily fails to teach accessing RAM blocks through a dedicated test bus as recited by Claim 11. Grider et al. does not remedy these deficiencies of Claim 11. For this additional reason, Claim 11 is allowable over Jamal in view of Grider et al.

Claims 12-18, which depend from Claim 11, are allowable over Jamal in view of Grider et al. for at least the same reasons as Claim 11.

In addition, Claim 12 recites "accessing the RAM blocks through dedicated test modules coupled to the test bus". As described above in connection with Claim 1, Jamal fails to teach or suggest more than one BIST unit. Thus, Jamal necessarily fails to teach accessing RAM blocks through dedicated test modules as recited by Claim 12. Grider et al. does not remedy this deficiency of Claim 12. For this additional reason, Claim 12 is allowable over Jamal in view of Grider et al.

In addition, Claim 13 recites, "storing a unique address in each of the test modules". Because Jamal only teaches the use of a single BIST unit (see above, discussion of Claim 8), Jamal necessarily fails to teach storing a unique address in a plurality of test modules as recited by Claim 13. Grider et al. does not remedy this deficiency of Claim 13. For this additional reason, Claim 13 is allowable over Jamal in view of Grider et al.

In addition, Claim 14 recites "coupling the pads to the system circuitry during normal operation of the chip; and coupling the pads to the test bus during the test mode."

In rejecting this claim, the Examiner refers to a section of Jamal that states "multiplexers provide paths from IC input/output (I/O) pads to the targeted subcircuit". (Jamal, Col. 1, lines 18 20.) However, Jamal fails to teach or suggest that these multiplexers are used to couple the same pads to system circuitry during normal operation, and to a test bus during a test mode. For this additional reason, Claim 14 is allowable over Jamal in view of Grider et al.

In addition, Claim 16 recites "writing test data values to the RAM blocks by broadcasting the test data values to all of the RAM blocks on the test bus". As described above in connection with Claim 1, Jamal fails to teach more than one RAM block. Thus, Jamal necessarily fails to teach or suggest "broadcasting the test data values to all of the RAM blocks on the test bus" as recited by Claim 16. Grider et al. fails to remedy the deficiencies of Jamal. For this additional reason, Claim 16 is allowable over Jamal in view of Grider et al.

In addition, Claim 18 recites "operating the test bus in response to a first clock signal during the test mode; and operating the RAM blocks in response to a second clock signal during the test mode, wherein the first clock signal and the second clock signal are independent signals".

As indicated by the Examiner, Jamal teaches "the test clock signal clocks the BIST circuitry 12 and testing operations performed by the BIST on the RAM 14". (Jamal, Col. 1, lines 46-48.) Because Jamal explicitly teaches using the test clock signal to clock both the BIST circuitry

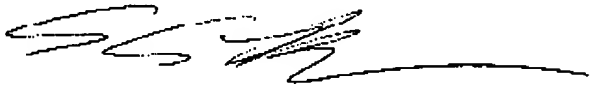
12 and the RAM 14, Jamal teaches away from "operating the test bus in response to a first clock signal during the test mode; and operating the RAM blocks in response to a second clock signal during the test mode, wherein the first clock signal and the second clock signal are independent signals" as recited by Claim 18. Grider et al. fails to remedy the deficiencies of Jamal. For this additional reason, Claim 18 is allowable over Jamal in view of Grider et al.

New Claim 19, which depends from Claim 18, recites "adjusting edges of the first clock signal relative to edges of the second clock signal". Support for Claim 19 appears in the specification as originally filed at paragraph [0067]. No new matter is added.

CONCLUSION

Claims 1-19 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If the Examiner has any questions or comments, he is invited to call the undersigned.

Respectfully submitted,



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